UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,657	03/11/2004	Stephen M. Prather	5298-13101 CD02212	6316

35617 7590 05/23/2005

DAFFER MCDANEIL LLP
P.O. BOX 684908
AUSTIN, TX 78768

EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,657	PRATHER ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-15 and 18-20* is/are rejected.

7)☒ Claim(s) *10,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, *the inverter comprises a p-channel transistor coupled in series with an n-channel transistor, a gate terminal coupled to the capacitor, the gate terminal of the p-channel transistor is coupled to a ground supply voltage and a gate terminal of the n-channel transistor is coupled to a power supply voltage, and the gate lengths and gate widts of the p-channel and n-channel transistors of the first and second inverters* must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Iida (U. S. PAT. 4,906,871).

In claim 1, Iida teaches all claimed features in Figs 3 and 5-7, a circuit, comprising: a differential amplifier (13); a capacitor (19) coupled to an output (a terminal coupled to a node at R3 opposite to Vcc) of the differential amplifier; an inverter (20) coupled to the capacitor; and a biasing circuit (Q7 or Q8) coupled between the capacitor and the inverter (as shown in Figs. 5-7).

In claim 2, Iida further teaches the circuit as recited in claim 1, wherein the inverter (20) comprises a p-channel transistor (Q5) coupled in series with an n-channel transistor (Q6).

In claim 3, Iida further teaches the circuit as recited in claim 1, the circuit as recited in claim 1, wherein the capacitor (19) comprises a pair of conductive terminals (terminals of 19) separated by a dielectric (inherent), and wherein a first terminal of the pair of terminals is coupled to the output (the terminal coupled to the node at R3

opposite to Vcc) of the differential amplifier and a second terminal of the pair of terminals is coupled to the inverter (20).

In claim 4, Iida further teaches the circuit as recited in claim 1, wherein the inverter (20) comprises a gate terminal (as shown) coupled to the capacitor (19).

In claim 5, Iida further teaches in Fig. 7, the circuit as recited in claim 1, wherein the biasing circuit comprises a transmission gate consisting of a p-channel transistor (Q8) coupled in parallel with an n- channel transistor (Q7).

In claim 6, Iida further teaches in Fig. 7, the circuit as recited in claim 5, wherein a gate terminal of the p-channel transistor (Q8) is coupled to a ground supply voltage (logic 0) and a gate terminal of the n-channel transistor (Q7) is coupled to a power supply voltage (Vcc or logic 1) during operation of the circuit.

In claim 7, Iida further teaches in Fig. 7, the circuit as recited in claim 5, wherein a gate terminal of the p-channel transistor is coupled to a power supply voltage (logic 1 turns off p-channel transistor) and a gate terminal of the n-channel transistor is coupled to a ground supply voltage (logic 0 turns of n-channel transistor) during power down of the circuit.

In claims 8 and 9, Iida further teaches in Fig. 8 the circuit as recited in claim 1, the circuit as recited in claim 1, wherein the biasing circuit comprises a second inverter (22); and wherein the second inverter comprises both an input and an output coupled to the capacitor (via R6).

Method claims 18-20 correspond to detailed circuitry already discussed similarly with regard to claims 1-9.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grossmann (U. S. PAT. 6,518,789) in view of Iida.

In claim 11, Grossmann teaches all claimed features in Fig. 1, a receiver, comprising: a pair of inverters (14, 15); a differential amplifier (Fig. 1) adapted to receive a differential input signal (9, 11) forwarded to the receiver from a transmission medium (differential line connected to 9 and 11, not shown); with the exception of teaching a biasing circuit coupled to an input of each of the pair of inverters to bias a voltage on the pair of inverters to a trip point of the inverters; and a pair of capacitors coupled between the pair of inverters and respective pair of outputs of the differential amplifier to place upon each of the pair of inverters changes in voltage centered around the trip point, wherein the changes in voltage correspond to changes in amplitude of the differential input signal. However, Iida teaches in Figs. 1 and 3-8, a biasing circuit (Q7) coupled to an input of each of the pair of inverters (only one of the inverters shown) to bias a voltage on the pair of inverters to a trip point (V1) of the inverters; and a pair of capacitors (only one of capacitors shown, 19) coupled between the pair of inverters and respective pair of outputs (only one of the outputs shown for simplicity) of the differential amplifier to place upon each of the pair of inverters changes in voltage centered around

the trip point (V1 in Fig. 4), wherein the changes in voltage correspond to changes in amplitude of the differential input signal.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Grossmann with the teachings of Iida in order to provide a differential CMOS level shifter circuit.

Claim 12, Iida further teaches the receiver as recited in claim 11, wherein each of the pair of inverters (only one of the inverter shown, 20) is a complementary metal oxide semiconductor (CMOS) inverter.

In claim 13, Iida further teaches the receiver as recited in claim 11, wherein the biasing circuit comprises a transmission gate (Q7 or Q8) coupled between the input and output of each of the pair of inverters to maintain a direct current (DC) voltage bias on the input of each of the pair of inverters approximately at the trip point (V1) of the inverters.

In claim 14, Iida further teaches the receiver as recited in claim 11, wherein the transmission gate comprises a p-channel transistor (Q8) coupled in parallel with an n-channel transistor (Q7), wherein, during operation, a gate terminal of the p-channel transistor is coupled to a ground supply voltage (logic 0 turns ON p-channel transistor) and a gate terminal of the n-channel is coupled to a power supply voltage (logic 1 turns on n-channel transistor), and wherein during non-operation, the gate terminal of the p-channel transistor is coupled to the power supply voltage (logic 1) and a gate terminal of the n-channel is coupled to the ground supply voltage (logic 0).

6. In claim 15, Iida further teaches the receiver as recited in claim 11, wherein the biasing circuit comprises a second inverter (22) having an input coupled to an output of the inverter and also having an output coupled to an input of the inverter (as shown in Fig. 8).

7. Claims 10, 16 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER